CLAIMS

1. A semiconductor device comprising one or two semiconductor chips, each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

a second electrostatic protection element provided in vicinity of said wiring; and

a fuse provided between said wiring and said second electrostatic protection element, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said second electrostatic protection element are connected to each other through said fuse, and

when said semiconductor device has said two semiconductor chips, said fuse is disconnected so that said second electrostatic protection element is electrically disconnected from said wiring.

2. A semiconductor device comprising one or two semiconductor chips, each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first and second electrostatic protection elements provided in vicinity of said wiring; and

first and second fuses provided between said wiring and said first and second electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first and second electrostatic protection elements are connected to each other through said fuses, and

when said semiconductor device has said two semiconductor chips, said first or second fuse is disconnected so that said first or second electrostatic protection element is electrically disconnected from said wiring.

3. A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of n, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

second to n-th electrostatic protection elements provided in vicinity of said wiring; and

second to n-th fuses provided between said wiring and said second to n-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said second to n-th electrostatic protection elements are connected to each other through said fuses, and

when said semiconductor device has said semiconductor chips in the number of n, said second to n-th fuses are disconnected so that said second to n-th electrostatic protection elements are electrically disconnected from said wiring, wherein said n is an integer more than two.

4. A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of n, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first and n-th electrostatic protection elements provided in vicinity of said wiring; and

first and n-th fuses provided between said wiring and said first and n-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to n-th electrostatic protection elements are connected to each other through said fuses, and

when said semiconductor device has said semiconductor chips in the number of n, said second to n-th fuses are disconnected so that said first electrostatic protection element is electrically connected to and said second to n-th electrostatic protection elements are electrically disconnected from said wiring, wherein said n is an integer more than two.

5. A semiconductor device comprising one semiconductor chip or a plurality of semiconductor chips, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a plurality of electrostatic protection elements provided in vicinity of said wiring; and

a plurality of fuses one each provided between said wiring and said electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and all of said electrostatic protection elements are connected to each other through said fuses, and

when said semiconductor device has said plurality of semiconductor chips, a predetermined number of said fuses are disconnected so that said electrostatic protection elements corresponding to said disconnected fuses are electrically disconnected from said wiring.

6. A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o or p, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

second to m-th electrostatic protection elements provided in vicinity of said wiring; and

second to m-th fuses provided between said wiring and said second to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to m-th electrostatic protection elements are connected to each other, and

when said semiconductor device has said semiconductor chips in the number of o, a first predetermined fuses of said m-th fuses are disconnected so that said first to (m/o)-th electrostatic protection

elements are electrically connected to and said (m/o + 1)th to m-th electrostatic protection elements are disconnected from said wiring,

when said semiconductor device has said semiconductor chips in the number of p, a second predetermined fuses of said m-th fuses are disconnected so that said first to (m/p)-th electrostatic protection elements are electrically connected to and said (m/p + 1)th to m-th electrostatic protection elements are disconnected from said wiring, wherein said o and p are integers more than 2 and said m is the lowest common multiple of said o and p.

7. A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o or p, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first to m-th electrostatic protection elements provided in vicinity of said wiring; and

first to m-th fuses provided between said wiring and said first to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to m-th electrostatic protection elements are connected to each other through said fuses, and

when said semiconductor device has said semiconductor chips in the number of o, a first predetermined fuses of said m-th fuses are disconnected so that said first to (m/o)-th electrostatic protection elements are electrically connected to and said (m/o + 1)th

to m-th electrostatic protection elements are disconnected from said wiring,

when said semiconductor device has said semiconductor chips in the number of p, a second predetermined fuses of said m-th fuses are disconnected so that said first to (m/p)-th electrostatic protection elements are electrically connected to and said (m/p + 1)th to m-th electrostatic protection elements are disconnected from said wiring, wherein said o and p are integers more than 2 and said m is the lowest common multiple of said o and p.

8. A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o, p, or q, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

second to m-th electrostatic protection elements provided in vicinity of said wiring; and

second to m-th fuses provided between said wiring and said second to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to m-th electrostatic protection elements are connected to each other, and

when said semiconductor device has said semiconductor chips in the number of o, a first predetermined fuses of said m-th fuses are disconnected so that said first to (m/o)-th electrostatic protection elements are electrically connected to and said (m/o + 1)th

to m-th electrostatic protection elements are disconnected from said wiring,

when said semiconductor device has said semiconductor chips in the number of p, a second predetermined fuses of said m-th fuses are disconnected so that said first to (m/p)-th electrostatic protection elements are electrically connected to and said (m/p + 1)th to m-th electrostatic protection elements are disconnected from said wiring,

when said semiconductor device has said semiconductor chips in the number of q, a third predetermined fuses of said m-th fuses are disconnected so that said first to (m/q)-th electrostatic protection elements are electrically connected to and said (m/q + 1)th to m-th electrostatic protection elements are disconnected from said wiring, wherein said o, p, and q are integers more than 2 and said m is the lowest common multiple of said o, p, and q.

9. A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o, p, or q, said semiconductor chip or each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first to m-th electrostatic protection elements provided in vicinity of said wiring; and

first to m-th fuses provided between said wiring and said first to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to m-th electrostatic protection elements are connected to each other through said fuses, and

when said semiconductor device has said semiconductor chips in the number of o, a first predetermined fuses of said m-th fuses are disconnected so that said first to (m/o)-th electrostatic protection elements are electrically connected to and said (m/o + 1)th to m-th electrostatic protection elements are disconnected from said wiring,

when said semiconductor device has said semiconductor chips in the number of p, a second predetermined fuses of said m-th fuses are disconnected so that said first to (m/p)-th electrostatic protection elements are electrically connected to and said (m/p + 1)th to m-th electrostatic protection elements are disconnected from said wiring,

when said semiconductor device has said semiconductor chips in the number of q, a third predetermined fuses of said m-th fuses are disconnected so that said first to (m/q)-th electrostatic protection elements are electrically connected to and said (m/q + 1)th to m-th electrostatic protection elements are disconnected from said wiring, wherein said o, p, and q are integers more than 2 and said m is the lowest common multiple of said o, p, and q.

10. The semiconductor device according to claim 1, wherein said first and second electrostatic protection elements are capacitors formed by MOS transistors.

11. The semiconductor device according to claim 2, wherein said first and second electrostatic protection elements are capacitors formed by MOS transistors.

12. The semiconductor device according to claim 3, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

13. The semiconductor device according to claim 4, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

14. The semiconductor device according to claim 5, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

15. The semiconductor device according to claim 6, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

16. The semiconductor device according to claim 7, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

17. The semiconductor device according to claim 8, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

18. The semiconductor device according to claim 9, wherein said electrostatic protection elements are capacitors formed by MOS transistors.

19. A method of setting a capacity of an input pin of said semiconductor device according to claim 1, comprising the step of disconnecting said fuse of said semiconductor chip to control said capacity.

20. A method of setting an input pin capacity of said semiconductor device according to claim 2, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

21. A method of setting an input pin capacity of said semiconductor device according to claim 3, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

22. A method of setting an input pin capacity of said semiconductor device according to claim 4, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

23. A method of setting an input pin capacity of said semiconductor device according to claim 5, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

24. A method of setting an input pin capacity of said semiconductor device according to claim 6, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

25. A method of setting an input pin capacity of said semiconductor device according to claim 7, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

26. A method of setting an input pin capacity of said semiconductor device according to claim 8, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

27. A method of setting an input pin capacity of said semiconductor device according to claim 9, comprising the step of disconnecting said fuses of said semiconductor chip to control said capacity.

28. The method according to claim 21, wherein said disconnecting of said fuses is performed according to a number of said semiconductor chips included in said semiconductor device.

29. The method according to claim 22, wherein said disconnecting of said fuses is performed according to a number of said semiconductor chips included in said semiconductor device.

30. The method according to claim 23, wherein said disconnecting of said fuses is performed according to a number of said semiconductor chips included in said semiconductor device.

31. The method according to claim 24, wherein said disconnecting of said fuses is performed according to

a number of said semiconductor chips included in said semiconductor device.

32. The method according to claim 25, wherein said disconnecting of said fuses is performed according to a number of said semiconductor chips included in said semiconductor device.

33. The method according to claim 26, wherein said disconnecting of said fuses is performed according to a number of said semiconductor chips included in said semiconductor device.

34. The method according to claim 27, wherein said disconnecting of said fuses is performed according to a number of said semiconductor chips included in said semiconductor device.

35. The method according to claim 19, wherein said disconnecting of said fuse is performed by laser.

36. The method according to claim 20, wherein said disconnecting of said fuses is performed by laser.

37. The method according to claim 21, wherein said disconnecting of said fuses is performed by laser.

38. The method according to claim 22, wherein said disconnecting of said fuses is performed by laser.

39. The method according to claim 23, wherein said disconnecting of said fuses is performed by laser.

40. The method according to claim 24, wherein said disconnecting of said fuses is performed by laser.

41. The method according to claim 25, wherein said disconnecting of said fuses is performed by laser.

42. The method according to claim 26, wherein said disconnecting of said fuses is performed by laser.

43. The method according to claim 27, wherein said disconnecting of said fuses is performed by laser.